

**What Is Claimed Is:**

1        1. A method for quantifying a number of identical consecutive digits  
2 starting from a fixed position within a string of  $n$  digits, comprising:

3              converting the string of  $n$  digits into a thermometer code, wherein the  
4 thermometer code uses  $m$  bits to represent a string of  $m$  identical consecutive  
5 digits within the string of  $n$  digits;

6              converting the thermometer code into a one-hot code in which only one bit  
7 has a logical one value; and

8              converting the one-hot code into a logarithmic code representing the  
9 number of identical consecutive digits.

1        2. The method of claim 1, wherein converting the string of digits into  
2 the thermometer code involves passing the string of digits through  $\lceil \log_2 n \rceil$  layers  
3 of AND gates, wherein a first layer of AND gates produces thermometer codes for  
4 sub-strings of length two, and wherein each consecutive layer produces  
5 thermometer codes for sub-strings of length  $k+1$  to  $2k$  by ANDing together  
6 thermometer codes for sub-strings of length 1 to  $k$  from preceding layers.

1        3. The method of claim 1,  
2 wherein converting the thermometer code into the one-hot code involves

3 passing the thermometer code through a single layer of two-input comparator  
4 gates;

5              wherein a given comparator gate produces a logical one value when a first  
6 input of the comparator gate receives a logical one value and a second input  
7 receives a logical zero value; and

8       wherein a comparator gate is coupled between each consecutive pair of  
9   thermometer code bits, so that only one comparator gate, covering a boundary  
10   between consecutive logical ones and consecutive logical zeros, produces a  
11   logical one value.

1           4.       The method of claim 1, wherein converting the one-hot code into  
2   the logarithmic code involves passing the one-hot code through  $\lceil \log_2 n \rceil - 1$  layers  
3   of OR gates, wherein a given bit in the logarithmic code is produced by ORing  
4   together bits of the one-hot code that cause the given bit in the logarithmic code to  
5   be asserted.

1           5.       The method of claim 1, wherein the string of  $n$  digits is a string of  
2    $n$  binary digits.

1           6.       The method of claim 1, wherein the fixed position in the string of  $n$   
2   digits is the beginning of the string, so that the number of leading identical  
3   consecutive digits is quantified.

1           7.       The method of claim 6, wherein the number of leading zero values  
2   is quantified.

1           8.       The method of claim 7, further comprising using the logarithmic  
2   code to normalize a result of a floating-point arithmetic operation.

1           9.       The method of claim 1, further comprising using the logarithmic  
2   code to encode or decode a stream of data, wherein the logarithmic code  
3   represents a run-length of identical consecutive digits within the stream of data.

1           10.     The method of claim 1, wherein each digit in the string of  $n$  digits  
2     includes one or more binary digits.

1           11.     An apparatus that quantifies a number of identical consecutive  
2     digits starting from a fixed position within a string of  $n$  digits, comprising:  
3                 a thermometer code circuit that converts the string of  $n$  digits into a  
4     thermometer code, wherein the thermometer code uses  $m$  bits to represent a string  
5     of  $m$  identical consecutive digits within the string of  $n$  digits;  
6                 a one-hot code circuit that converts the thermometer code into a one-hot  
7     code in which only one bit has a logical one value; and  
8                 a logarithmic code circuit that converts the one-hot code into a logarithmic  
9     code representing the number of identical consecutive digits.

1           12.     The apparatus of claim 11, wherein the thermometer code circuit  
2     includes  $\lceil \log_2 n \rceil$  layers of AND gates, wherein a first layer of AND gates produces  
3     thermometer codes for sub-strings of length two, and wherein each consecutive  
4     layer produces thermometer codes for sub-strings of length  $k+1$  to  $2k$  by ANDing  
5     together thermometer codes for sub-strings of length 1 to  $k$  from preceding layers.

1           13.     The apparatus of claim 11,  
2                 wherein the one-hot-code circuit includes a single layer of two-input  
3     comparator gates;  
4                 wherein a given comparator gate produces a logical one value when a first  
5     input of the comparator gate receives a logical one value and a second input  
6     receives a logical zero value; and

7           wherein a comparator gate is coupled between each consecutive pair of  
8   thermometer code bits, so that only one comparator gate, covering a boundary  
9   between consecutive logical ones and consecutive logical zeros, produces a  
10   logical one value.

1           14.     The apparatus of claim 11, wherein the logarithmic code circuit  
2   includes  $\lceil \log_2 n \rceil - 1$  layers of OR gates, wherein a given bit in the logarithmic code  
3   is produced by ORing together bits of the one-hot code that cause the given bit in  
4   the logarithmic code to be asserted.

1           15.     The apparatus of claim 11, wherein the string of  $n$  digits is a string  
2   of  $n$  binary digits.

1           16.     The apparatus of claim 11, wherein the fixed position in the string  
2   of  $n$  digits is the beginning of the string, so that the number of leading identical  
3   consecutive digits is quantified.

1           17.     The apparatus of claim 16, wherein the apparatus quantifies the  
2   number of leading zero values.

1           18.     The apparatus of claim 17, further comprising a floating-point  
2   arithmetic unit that is configured to use the logarithmic code to normalize a result  
3   of a floating-point arithmetic operation.

1           19.     The apparatus of claim 11, further comprising an encoder that is  
2   configured to use the logarithmic code to encode or decode a stream of data,

1 wherein the logarithmic code represents a run-length of identical consecutive  
2 digits within the stream of data.

1           20. The apparatus of claim 11, wherein each digit in the string of  $n$   
2 digits includes one or more binary digits.

1           21. A computer system including a circuit that quantifies a number of  
2 identical consecutive digits, comprising:

3           a processor;

4           a memory;

5           a quantifying circuit that quantifies the number of identical consecutive  
6 digits starting from a fixed position within a string of  $n$  digits, wherein the  
7 quantifying circuit includes,

8                 a thermometer code circuit that converts the string of  $n$   
9                 digits into a thermometer code, wherein the thermometer code uses  
10                  $m$  bits to represent a string of  $m$  identical consecutive digits within  
11                 the string of  $n$  digits;

12                 a one-hot code circuit that converts the thermometer code  
13                 into a one-hot code in which only one bit has a logical one value,  
14                 and

15                 a logarithmic code circuit that converts the one-hot code  
16                 into a logarithmic code representing the number of identical  
17                 consecutive digits.

1           22. The computer system of claim 21, further comprising:  
2                 a floating-point arithmetic unit of within the processor;

3           wherein the quantifying circuit is located within the floating-point  
4 arithmetic unit and is configured to normalize results of floating-point operations.

1           23.     The computer system of claim 21,  
2           wherein the computer system includes an encoding circuit for encoding or  
3 decoding streams of data; and  
4           wherein the quantifying circuit is located within the encoding circuit and is  
5 configured to quantify run-lengths of identical consecutive digits for the encoding  
6 circuit.